



# TPS82084 2-A High Efficiency Step-Down Converter MicroSiP™ with Integrated Inductor

## 1 Features

- 2-A, Low Profile MicroSiP™ Power Module
- DCS-Control™ Topology
- Up to 95% Efficiency
- 17- $\mu$ A Operating Quiescent Current
- -40°C to 125°C Operating Temperature Range
- Hiccup Short Circuit Protection
- 2.5-V to 6-V Input Voltage Range
- 0.8-V to  $V_{IN}$  Adjustable Output Voltage
- Power Save Mode for Light Load Efficiency
- 100% Duty Cycle for Lowest Dropout
- Output Discharge Function
- Power Good Output
- Integrated Soft Startup
- Over Temperature Protection
- 3.0-mm x 2.8-mm x 1.3-mm 8-Pin  $\mu$ SiL Package

## 2 Applications

- Battery Powered Applications
- Solid State Drives
- Processor Supply
- Mobile Phones

## 3 Description

The TPS82084 device is a 2-A step-down converter MicroSiP™ module optimized for small solution size and high efficiency. The power module integrates a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 2.4MHz and automatically enters Power Save Mode operation at light load currents. In Power Save Mode, the device operates with typically 17- $\mu$ A quiescent current. Using the DCS-Control™ topology, the device achieves excellent load transient performance and accurate output voltage regulation. The EN and PG pins, which support sequencing configurations, bring a flexible system design. An integrated soft startup reduces the inrush current required from the input supply. Over temperature protection and Hiccup short circuit protection deliver a robust and reliable solution.

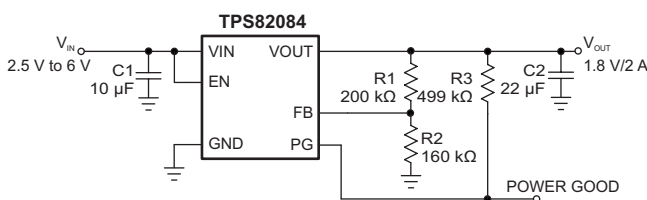
### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS82084	$\mu$ SiL (8)	3.00 mm x 2.80 mm

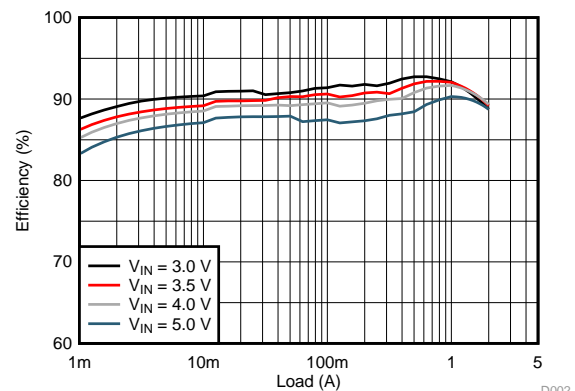
(1) For all available packages, see the orderable addendum at the end of the datasheet.

## 4 Simplified Schematic

### 1.8 V Output Application



### 1.8 V Output Efficiency



D002



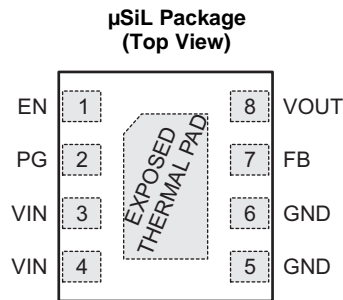
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## 5 Revision History

DATE	REVISION	NOTES
June 2015	*	Initial release.

## 6 Pin Configuration and Functions



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	1	I	Enable pin. Pull High to enable the device. Pull Low to disable the device. This pin has an internal pull-down resistor of typically 400 kΩ when the device is disabled.
PG	2	O	Power good open drain output pin. A pull-up resistor can be connected to any voltage less than 6V. Leave it open if it is not used.
VIN	3,4	PWR	Input voltage pin.
GND	5,6		Ground pin.
FB	7	I	Feedback reference pin. An external resistor divider connected to this pin programs the output voltage.
VOUT	8	PWR	Output voltage pin.
Exposed Thermal Pad			The exposed thermal pad must be connected to the GND pin. Must be soldered to achieve appropriate power dissipation and mechanical reliability.

**PRODUCT PREVIEW**

## 7 Specifications

### 7.1 Absolute Maximum Ratings<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage at pins <sup>(2)</sup>	EN, PG, VIN, FB, VOUT	-0.3	7	V
Sink current	PG		1.0	mA
Module operating temperature range		-40	125	°C
Storage temperature range		-40	125	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground pin.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommend Operating Conditions

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
V <sub>IN</sub>	Input voltage range	2.5	6	V
V <sub>PG</sub>	Power good pull-up resistor voltage		6	V
V <sub>OUT</sub>	Output voltage range	0.8	V <sub>IN</sub>	V
I <sub>OUT</sub>	Output current range <sup>(1)</sup>	0	2	A
T <sub>J</sub>	Module operating temperature range <sup>(1)</sup>	-40	125	°C

- (1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated.

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS82084	UNIT
		μSiL	
		8-Pin	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	68.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	n/a	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	n/a	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.4	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	30.0	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	n/a	°C/W

- (1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, [SPRA953](#)

## 7.5 Electrical Characteristics

$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $V_{IN} = 2.5\text{V}$  to  $6\text{V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{IN} = 3.6\text{V}$ , unless otherwise noted.

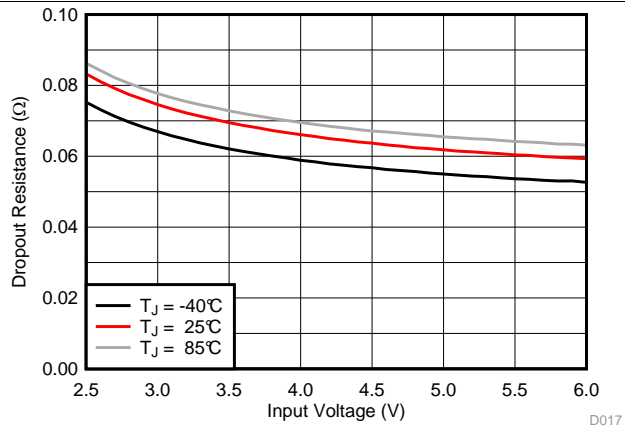
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$V_{IN}$	Input voltage range		2.5		6	V
$I_Q$	Quiescent current into $V_{IN}$	No load, device not switching $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ , $V_{IN} = 2.5\text{V}$ to $5.5\text{V}$		17	25	$\mu\text{A}$
$I_{SD}$	Shutdown current into $V_{IN}$	EN = Low, $T_J = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$ , $V_{IN} = 2.5\text{V}$ to $5.5\text{V}$		0.7	5	$\mu\text{A}$
$V_{UVLO}$	Under voltage lock out threshold	$V_{IN}$ falling	2.1	2.2	2.3	V
		$V_{IN}$ rising	2.3	2.4	2.5	V
$T_{JSD}$	Thermal shutdown threshold	$T_J$ rising		150		$^{\circ}\text{C}$
	Thermal shutdown hysteresis	$T_J$ falling		20		$^{\circ}\text{C}$
<b>LOGIC INTERFACE EN</b>						
$V_{IH}$	High-level input voltage		1.0	0.8		V
$V_{IL}$	Low-level input voltage			0.7	0.4	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High		0.01	0.16	$\mu\text{A}$
$R_{PD}$	Pull-down resistance at EN pin	EN = Low		400		k $\Omega$
<b>SOFT START, POWER GOOD</b>						
$V_{PG}$	Power good threshold	$V_{OUT}$ rising, referenced to $V_{OUT}$ nominal	93%	95%	98%	
		$V_{OUT}$ falling, referenced to $V_{OUT}$ nominal	88%	90%	93%	
$V_{PG,OL}$	Low-level output voltage	$I_{sink} = 1\text{mA}$			0.4	V
$I_{lkg(PG)}$	Input leakage current into PG pin	$V_{PG} = 5\text{V}$		0.01	0.16	$\mu\text{A}$
<b>OUTPUT</b>						
$V_{OUT}$	Output voltage range		0.8		$V_{IN}$	V
$V_{FB}$	Feedback regulation voltage	PWM mode	792	800	808	mV
		PSM mode, $C_{OUT} = 22\text{ }\mu\text{F}$	792	800	817	
$I_{lkg(FB)}$	Feedback input leakage current	$V_{FB} = 0.8\text{V}$		0.01	0.1	$\mu\text{A}$
$R_{DIS}$	Output discharge resistor	EN = Low, $V_{OUT} = 1.8\text{V}$		260		$\Omega$
	Line regulation	$I_{OUT} = 1\text{A}$ , $V_{IN} = 2.5\text{V}$ to $6\text{V}$		0.02		%/V
	Load regulation	$I_{OUT} = 0.5\text{A}$ to $2\text{A}$		0.16		%/A
<b>POWER SWITCH</b>						
$R_{DS(on)}$	High-side FET on-resistance	$I_{SW} = 500\text{mA}$		31	56	m $\Omega$
	Low-side FET on-resistance	$I_{SW} = 500\text{mA}$		23	45	m $\Omega$
$R_{DP}$	Dropout resistance	100% mode		69		m $\Omega$
$I_{LIMF}$	High-side FET switch current limit			3.6		A
$f_{SW}$	PWM switching frequency	$I_{OUT} = 1\text{A}$		2.4		MHz

## 7.6 Timing Requirements

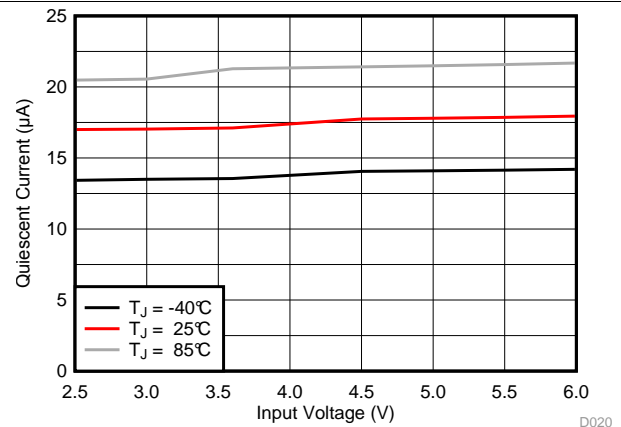
$T_J = -40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  and  $V_{IN} = 2.5\text{V}$  to  $6\text{V}$ . Typical values are at  $T_J = 25^{\circ}\text{C}$  and  $V_{IN} = 3.6\text{V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SOFT START</b>						
$t_{SS}$	Soft start time	Time from EN high to 95% of $V_{OUT}$ nominal		0.8		ms

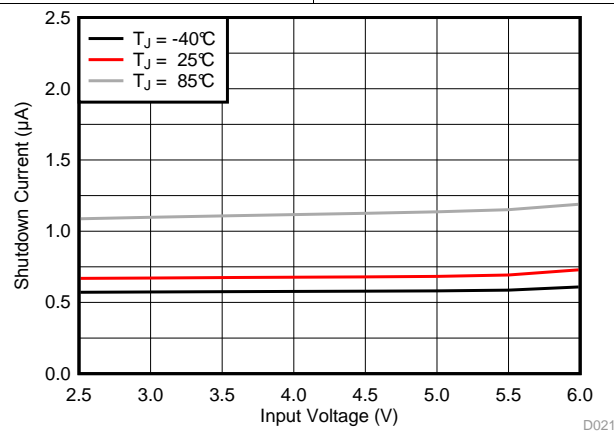
## 7.7 Typical Characteristics



**Figure 1. Dropout Resistance**



**Figure 2. Quiescent Current**



**Figure 3. Shutdown Current**

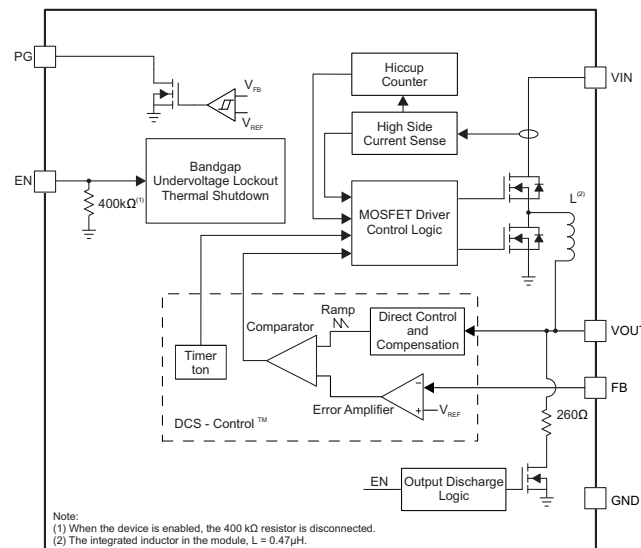
## 8 Detailed Description

### 8.1 Overview

The TPS82084 synchronous step-down converter power module is based on DCS-Control™ (Direct Control with Seamless transition into Power Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic, voltage and current mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power Save Mode) at light load currents. In PWM, the converter operates with its nominal switching frequency of 2.4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPS82084 offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 PWM and PSM Operation

The TPS82084 includes a fixed on-time ( $t_{ON}$ ) circuitry. This  $t_{ON}$ , in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 420\text{ns} \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

In PWM mode, the TPS82084 operates with pulse width modulation in continuous conduction mode (CCM) with a  $t_{ON}$  shown in Equation 1 at medium and heavy load currents. A PWM switching frequency of typically 2.4 MHz is achieved by this  $t_{ON}$  circuitry. The device operates in PWM mode as long as the output current is higher than half the inductor's ripple current estimated by Equation 2.

$$\Delta I_L = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} \quad (2)$$

To maintain high efficiency at light loads, the device enters Power Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the inductor's ripple current. In PSM, the converter operates with a reduced switching frequency and with a minimum quiescent current to maintain high efficiency. The on time in PSM is also based on the same  $t_{ON}$  circuitry. The switching frequency in PSM is estimated as:

## Feature Description (continued)

$$f_{\text{PFM}} = \frac{2 \times I_{\text{OUT}}}{t_{\text{ON}}^2 \times \frac{V_{\text{IN}}}{V_{\text{OUT}}} \times \frac{V_{\text{IN}} - V_{\text{OUT}}}{L}} \quad (3)$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance. The output voltage accuracy in PSM operation is reflected in the electrical specification table and given for a 22-μF output capacitor.

### 8.3.2 Low Dropout Operation (100% Duty Cycle)

The device offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{\text{IN}(\text{min})} = V_{\text{OUT}(\text{min})} + I_{\text{OUT}} \times R_{\text{DP}}$$

where

- $R_{\text{DP}}$  = Resistance from  $V_{\text{IN}}$  to  $V_{\text{OUT}}$ , including high-side FET on-resistance and DC resistance of the inductor.
- $V_{\text{OUT}(\text{min})}$  = Minimum output voltage the load can accept.

### 8.3.3 Soft Startup

The TPS82084 has an internal soft start circuit which ramps up the output voltage to the nominal voltage during a soft start time of typically 0.8ms. This avoids excessive inrush current and creates a smooth output voltage slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance. The device is able to monotonically start into a pre-biased output capacitor. The device starts with the applied bias voltage and ramps the output voltage to its nominal value.

### 8.3.4 Switch Current Limit and Short Circuit Protection (Hiccup-Mode)

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a heavy load/shorted output circuit condition. If the inductor peak current reaches the switch current limit, the high-side FET is turned off and the low-side FET is turned on to ramp down the inductor current. Once this switch current limits is triggered 32 times, the devices stop switching and enables the output discharge. The devices then automatically start a new startup after a typical delay time of 66μs has passed. This is named HICCUP short circuit protection. The devices repeat this mode until the high load condition disappears.

### 8.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, an under voltage lockout is implemented, which shuts down the devices at voltages lower than  $V_{\text{UVLO}}$  with a hysteresis of 200 mV.

### 8.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops switching once the junction temperature exceeds  $T_{\text{JSD}}$ . Once the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically.



## 8.4 Device Functional Modes

### 8.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic High. Accordingly, shutdown mode is forced if the EN pin is pulled Low with a shutdown current of typically 0.7  $\mu$ A. An internal resistor of 260  $\Omega$  discharges the output via the VOUT pin smoothly when the device is disabled. The output discharge function also works when thermal shutdown, undervoltage lockout or short circuit protection are triggered.

An internal pull-down resistor of 400 k $\Omega$  is connected to the EN pin when the EN pin is Low. The pull-down resistor is disconnected when the EN pin is High.

### 8.4.2 Power Good Output

The device has a power good (PG) output. The PG pin goes high impedance once the output is above 95% of the nominal voltage, and is driven low once the output voltage falls below typically 90% of the nominal voltage. The PG pin is an open drain output and is specified to sink up to 1 mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 6 V.

The PG pin goes low when the device is disabled or in thermal shutdown. When the device is in UVLO, the PG pin is high impedance. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin floating when it is not used.

## 9 Application and Implementation

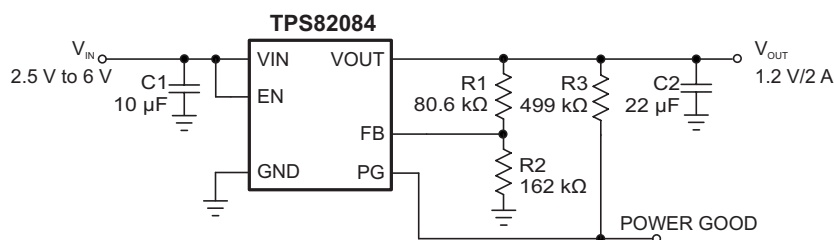
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The TPS82084 is a synchronous step-down converter power module whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design for several input and output voltage options by using typical applications as a reference.

### 9.2 Typical Applications



**Figure 4. 1.2-V Output Application**

#### 9.2.1 Design Requirements

For this design example, use the input parameters shown in [Table 1](#).

**Table 1. Design Parameters**

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.5 V to 6 V
Output voltage	1.2 V
Output ripple voltage	< 20 mV
Output current rating	2 A

[Table 2](#) lists the components used for the example.

**Table 2. List of Components<sup>(1)</sup>**

REFERENCE	DESCRIPTION	MANUFACTURER
C1	10 μF, Ceramic Capacitor, 10 V, X7R, size 0805, GRM21BR71A106KE51	Murata
C2	22 μF, Ceramic Capacitor, 6.3 V, X7R, size 0805, CL21B226MQQNNNE or 22 μF, Ceramic Capacitor, 6.3 V, X7S, size 0805, C2012X7S1A226M125AC	Samsung or TDK
R1	Depending on the output voltage, 1% accuracy	Std
R2	16 kΩ, 1% accuracy	Std
R3	499 kΩ, 1% accuracy	Std

(1) See [Third-Party Products](#) disclaimer

## 9.2.2 Detailed Design Procedure

### 9.2.2.1 Setting the Output Voltage

The output voltage is set by an external resistor divider according to the following equations:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right) = 0.8 \text{ V} \times \left(1 + \frac{R1}{R2}\right) \quad (5)$$

R2 should not be higher than 180 kΩ to achieve high efficiency at light load while providing acceptable noise sensitivity. Larger currents through R2 improve noise sensitivity and output voltage accuracy. [Figure 4](#) shows a recommended external resistor divider value for a 1.2-V output. Choose appropriate resistor values for other output voltages.

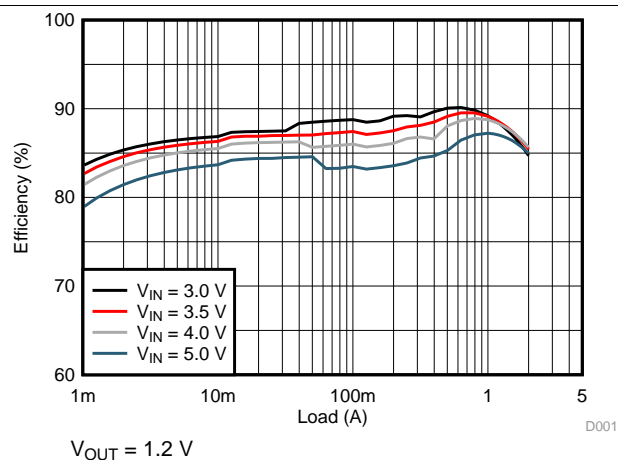
### 9.2.2.2 Input and Output Capacitor Selection

For best output and input voltage filtering, ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 10-μF or larger input capacitor is required. The output capacitor value can range from 22 μF up to more than 150 μF. The recommended typical output capacitor value is 22 μF. Values over 150 μF may be possible with a reduced load during startup in order to avoid triggering the Hiccup short circuit protection. A feed forward capacitor is not required for proper operation.

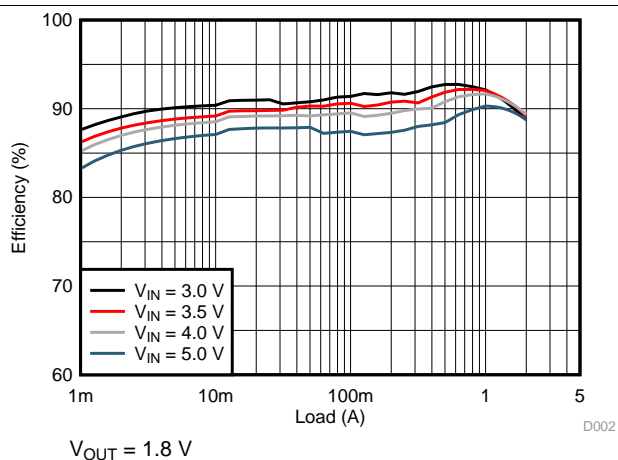
Ceramic capacitor has a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the input effective capacitance is at least 5 μF and the output effective capacitance is at least 8μF.

### 9.2.3 Application Performance Curves

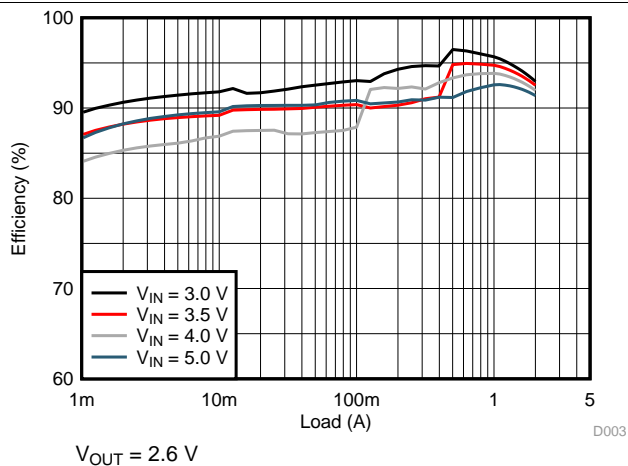
$T_A = 25^\circ\text{C}$ ,  $V_{IN} = 5\text{ V}$ ,  $V_{OUT} = 1.2\text{ V}$ , unless otherwise noted.



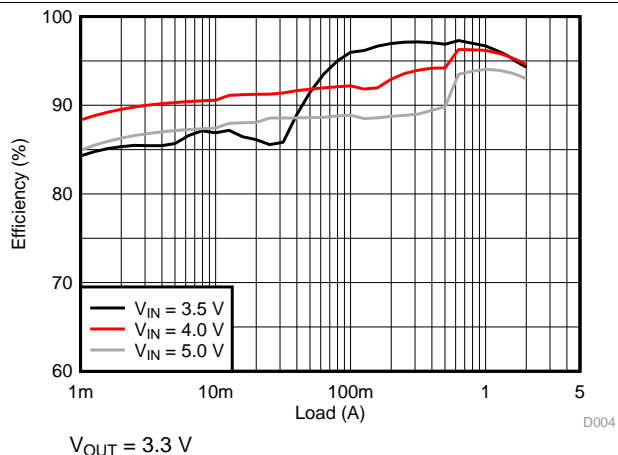
**Figure 5. Efficiency**



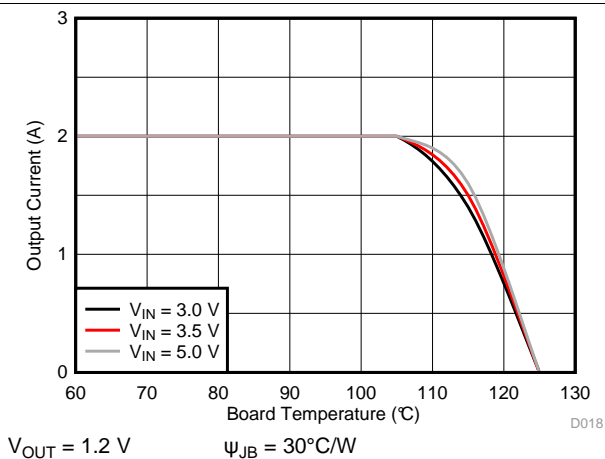
**Figure 6. Efficiency**



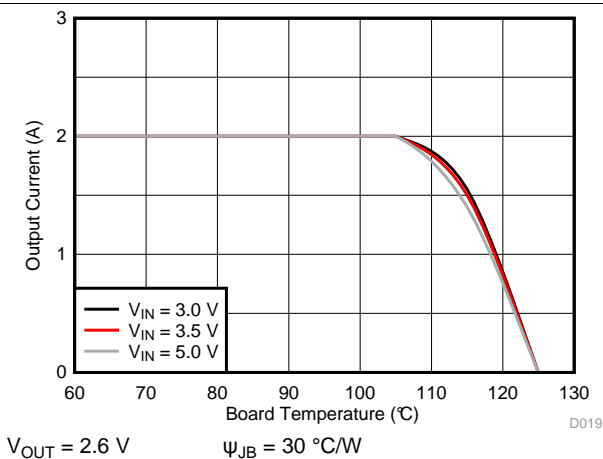
**Figure 7. Efficiency**



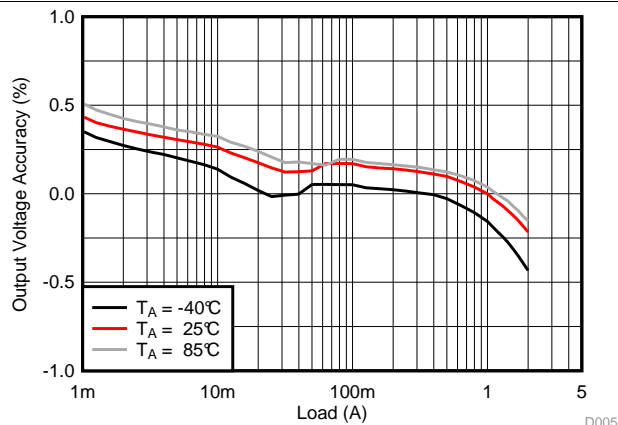
**Figure 8. Efficiency**



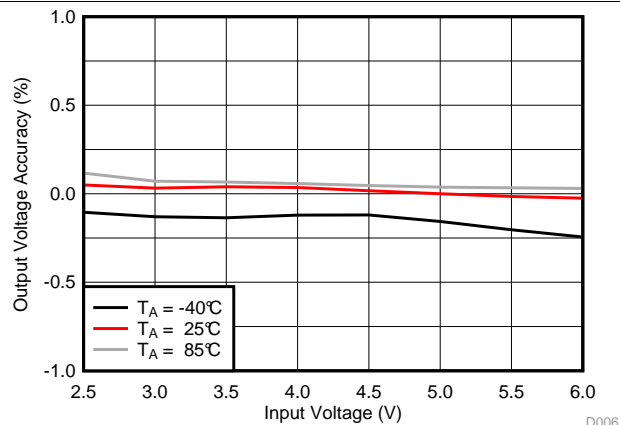
**Figure 9. Thermal Derating**



**Figure 10. Thermal Derating**

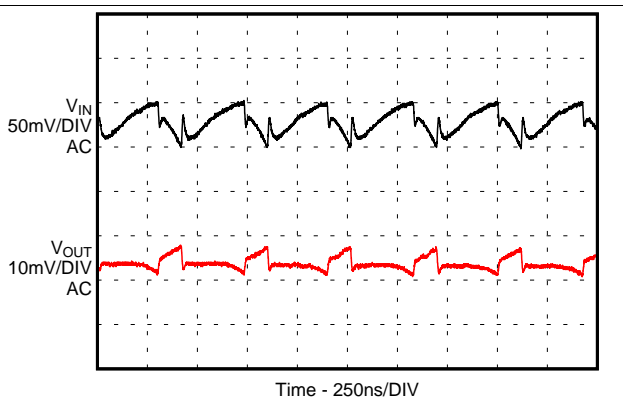


**Figure 11. Load Regulation**



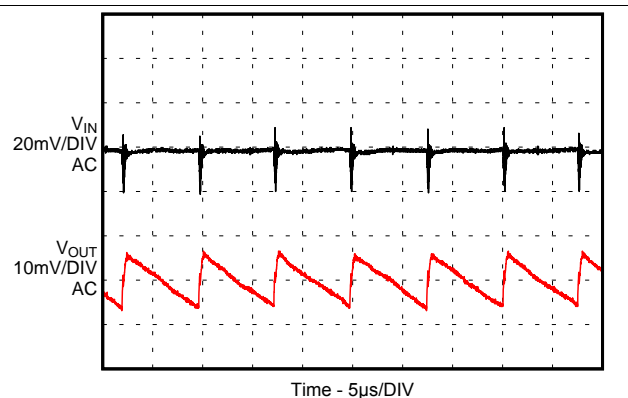
$I_{OUT} = 1\text{ A}$

**Figure 12. Line Regulation**



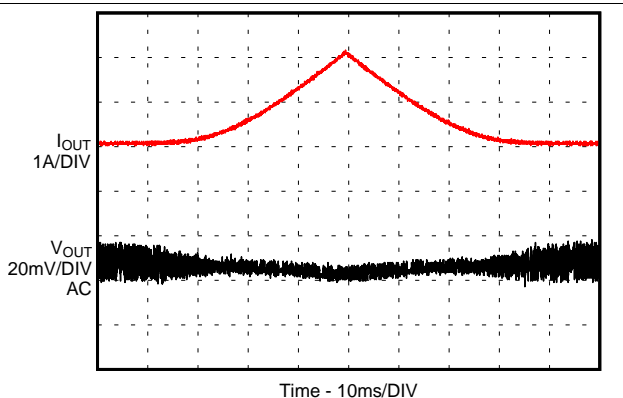
$I_{OUT} = 2\text{ A}$

**Figure 13. Input and Output Ripple in PWM Mode**



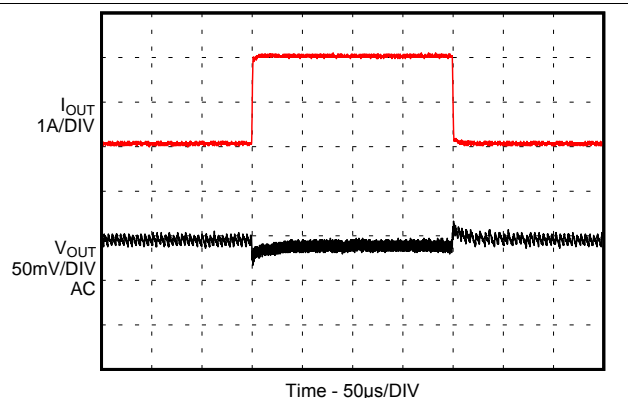
$I_{OUT} = 25\text{ mA}$

**Figure 14. Input and Output Ripple in PSM Mode**



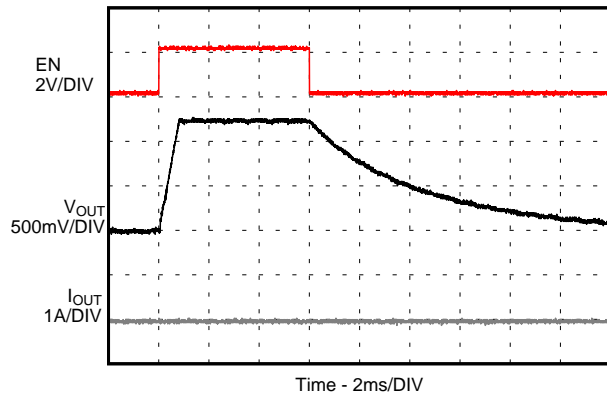
$I_{OUT} = 25\text{ mA to } 2\text{ A}$

**Figure 15. Load Sweep**



$I_{OUT} = 25\text{ mA to } 2\text{ A}$

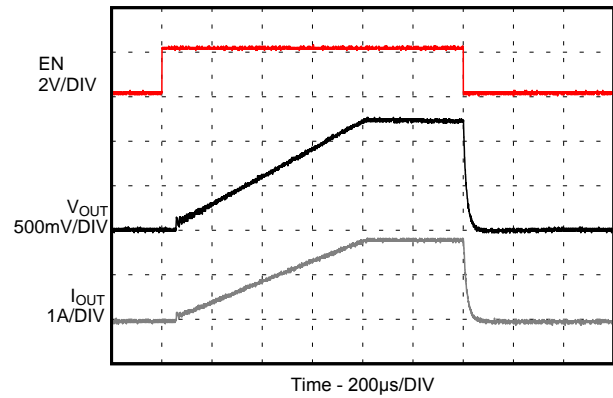
**Figure 16. Load Transient**



I<sub>OUT</sub> = no load

D012

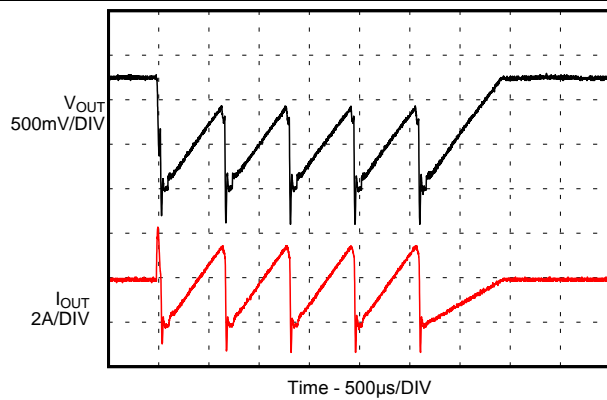
**Figure 17. Startup / Shutdown without Load**



Load = 0.68  $\Omega$

D013

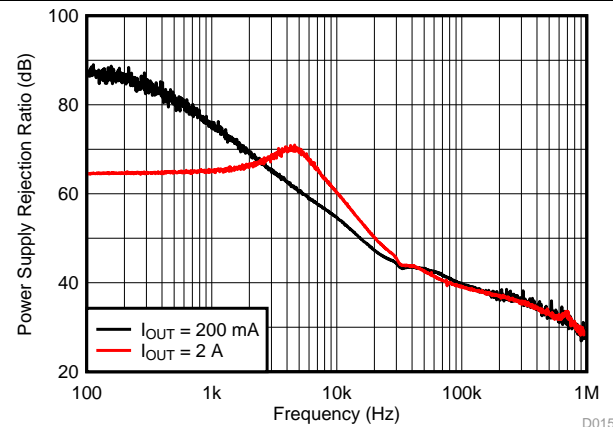
**Figure 18. Startup / Shutdown with Resistive Load**



I<sub>OUT</sub> = 2 A

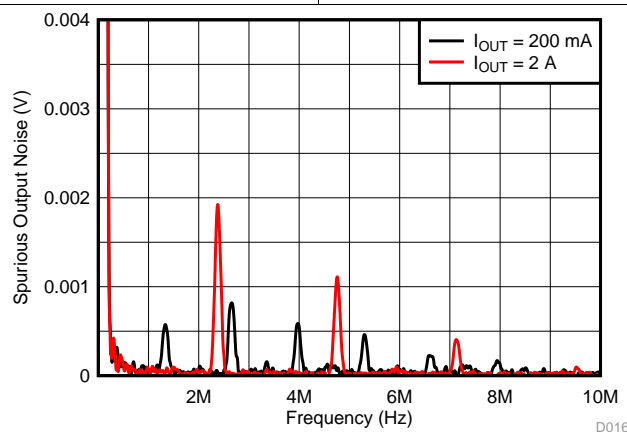
D014

**Figure 19. Short Circuit, HICCUP Protection Entry / Exit**



D015

**Figure 20. Power Supply Rejection Ratio (PSRR)**



D016

**Figure 21. Spurious Output Noise**

## 10 Power Supply Recommendations

The devices are designed to operate from an input supply voltage range between 2.5 V and 6 V. The average input current of the TPS82084 is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (6)$$

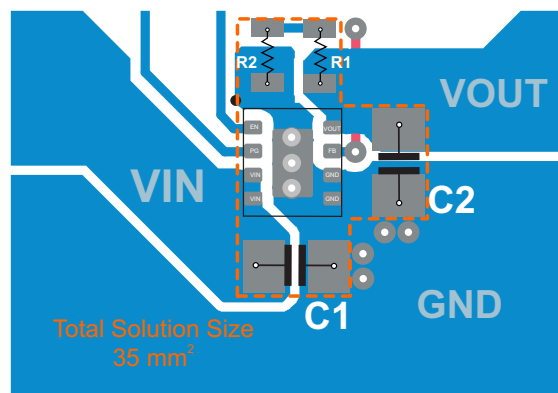
Ensure that the power supply has a sufficient current rating for the application.

## 11 Layout

### 11.1 Layout Guidelines

- It is recommended to place all components as close as possible to the IC. Specially, the input capacitor placement must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- To enhance heat dissipation of the device, the exposed thermal pad should be connected to bottom or internal layer ground planes using vias.
- Refer to [Figure 22](#) for an example of component placement, routing and thermal design.
- The recommended land pattern for the TPS82084 is shown at the end of this data sheet. For best manufacturing results, it is important to create the pads as solder mask defined (SMD). This keeps each pad the same size and avoids solder pulling the device during reflow.

### 11.2 Layout Example



**Figure 22. TPS82084 PCB Layout**

### 11.3 Thermal Consideration

The TPS82084's output current needs to be derating when the device operates in a high ambient temperature or deliver high output power. The amount of current derated is dependent upon the input voltage, output power, PCB layout design and environmental thermal condition. Care should especially be taken in applications where the localized PCB temperature exceeds 65°C.

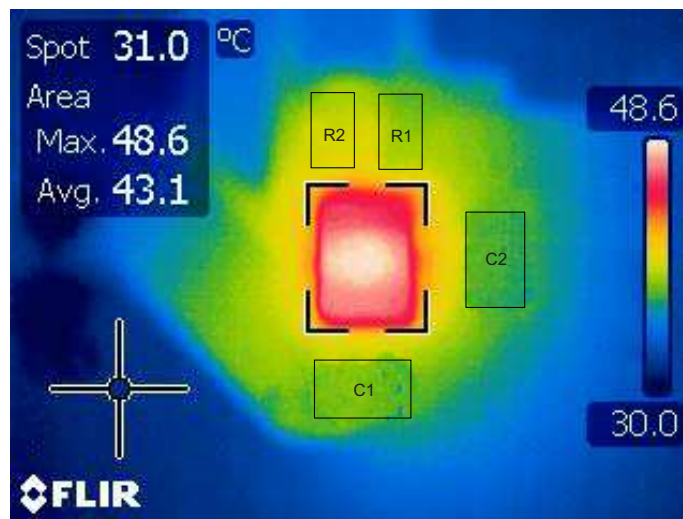
The TPS82084 module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate approximate module temperature of TPS82084, apply the typical efficiency stated in this datasheet to the desired application condition for the module power dissipation, then calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: [SZZA017](#) and [SPRA953](#).

Figure 23 shows the thermal measurement on the TPS82084EVM-672. It gives a guideline on the temperature rise when the TPS82084 is operated in free air at 25°C ambient under certain application conditions. The temperatures are checked at Spot and Area as listed below:

- Spot: temperature of the EVM board
- Area: temperature of the TPS82084



$$V_{IN} = 5 \text{ V}, V_{OUT} = 3.3 \text{ V}, I_{OUT} = 2 \text{ A}$$

**Figure 23. Thermal Measurement**



## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Third-Party Products Disclaimer

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### 12.2 Trademarks

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### 12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS82084SILR	PREVIEW	uSiP	SIL	8	3000	TBD	Call TI	Call TI	-40 to 125		
TPS82084SILT	PREVIEW	uSiP	SIL	8	250	TBD	Call TI	Call TI	-40 to 125		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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